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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,182	03/01/2005	Mark Thomas Johnson	NL 020838	7051

24737 7590 10/16/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
JOSEPH, DENNIS P	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,182	JOHNSON ET AL.	
	Examiner	Art Unit	
	Dennis P. Joseph	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/526,182.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to amendments filed in application No. 10/526,182 on August 22, 2007. Claims 1-8 are pending and have been examined.

Claim Rejections – 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5, 7 and 8** rejected under 35 U.S.C. 102(b) as being anticipated by **Shieh et al. (5,748,160)**

Shieh teaches in Claim 1:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") comprising

a matrix of display pixels being associated with intersections of crossing select electrodes and control electrodes (Column 3, Lines 39-45, "As is understood in the art, a scan signal is applied to each row for a sufficient time to allow all of the data drivers to be activated so that each pixel in the row being scanned is addressed. A scan signal is then applied to the next row

and all of the data drivers are activated, etc. Therefore, each pixel in the matrix is addressed with a scan and data signal by the combination of data drivers **25** and shift register **27**." From Figure 3, the control electrodes are from the data driver **55** and the select electrodes are from the shift register scan driver **57**.) ,

a select driver for supplying select signals (SE) to the select electrodes (Figure 3, the shift register scan driver **57** sends the select electrodes)

a control driver for supplying control signals (DA) to the control electrodes (Figure 3, the data driver **55** supplies the data signals.),

a voltage level generator for generating a plurality of different voltage levels (VBi) (Figure 3 shows the voltage source **60** with terminals V_R, V_G, and V_B), and

select circuits (Figure 3, switch **42**), each being coupled between an associated one of the display pixels and the voltage level generator for supplying a selected one of said plurality of different voltage levels (VBi) (Figure 5 shows the multi-step voltage waveforms for each of RGB) via at least one voltage level electrode (Figure 3 shows three voltage electrodes for each of the sub-pixels **45**, **46** and **47**) to the associated one of the display pixels in dependence on both the select signals (SE) indicating whether the associated one of the pixels is selected and a control signal (CG) being applied to said voltage level generator (Figure 3 shows a signal being sent from the timing circuit 65 to voltage source 60 to select the appropriate voltage (Columns 3-4, Lines 65-8) to indicate which one of said plurality of different voltage levels (VBi) has to be supplied to the associated one of the pixels. (Column 6, Lines 7-12, "In the multi-step voltage waveform of FIG. 5, one complete frame is illustrated. Each frame is divided into three subframes Vr, Vg, and Vb and each subframe is divided into m multi-steps of voltage or sub-

subframes. As described previously, the multi-step subframe Vr is applied to the Vr output of voltage source 60 and the entire **matrix** is addressed for each of the m steps. This procedure is continued until all m of the sub-subframes are completed, completing a subframe." The matrix setup uses information from both the select and control electrodes.)

Shieh teaches in Claim 2:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") as claimed in claim 1, characterized in that said voltage level generator (Figure 3, voltage source **60**) is adapted for supplying the plurality of different voltage levels (VBi) as a single voltage signal (VB) having different levels occurring successively in time during select periods (TS) (Figure 5 shows the multi-step waveform which is a signal voltage signal with a plurality of different voltage levels), and in that the select driver is adapted for selecting the associated one of the pixels during each of the select periods (TS) (Column 4, Lines 53-55, "In the structure of FIG. 3, for purposes of this explanation, a shift register **57** is provided to supply the scan signals."), the control signal (DA) determining whether a particular one of the plurality of different voltage levels (VBi) is supplied to the associated one of the pixels. (Figure 3 shows the data driver which is responsible for this input and is sent to the sub-pixels **45-47**.)

Shieh teaches in Claim 3:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") as claimed in claim 2, characterized in that the select circuits (Figure 3, **42**) each comprise

a single drive switch having a main current path coupled between the associated one of the pixels and a single voltage level electrode carrying the single voltage signal (VB) (Figure 3 shows the drive transistor **43**), and

a single select switch (Figure 3, **50**) having a main current path being arranged between one of the control electrodes and a control input of said single drive switch, and having a control input coupled to one of the select electrodes. (Column 4, Lines 23-25, "Switch **42** further includes a second transistor **50** having a current carrying terminal **51** connected to a gate or control terminal **52** of transistor **43**." The select transistor conveys the current to the drive transistor of the sub-pixels.)

Shieh teaches in Claim 4:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") as claimed in claim 1, characterized in that said voltage level generator is adapted for supplying at least two voltage signals (VBA, VBB) each comprising at least one of the plurality of different voltage levels (VBi) (Figure 5 shows the multi-step waveform with at least two voltage signals and these are applied from voltage source **60**.), and in that the select

driver is adapted for selecting the associated one of the pixels during each select period (TS) (Column 4, Lines 53-55, "In the structure of FIG. 3, for purposes of this explanation, a shift register **57** is provided to supply the scan signals."), the control signal (DA) determining whether one of the at least two voltage signals (VBA, VBB) is supplied to the associated one of the pixels. (Figure 3 shows the data driver which is responsible for this input.)

Shieh teaches in Claim 5:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") as claimed in claim 4, characterized in that said matrix display comprises at least two voltage level electrodes, each for carrying one of the at least two voltage signals (VBA, VBB) (Figure 3 shows the sub-pixels **45-47** which have voltages across them),

the select driver (Figure 3, shift register scan **57**) comprises

a plurality of drive switches, each having a main current path coupled between the associated one of the pixels and one of the at least two voltage level electrodes (Figure 3 shows the drive transistor **43**. This is a matrix setup and is a simplified diagram showing one pixel), and

a plurality of select switches (Figure 3, **50**), each being coupled between a same one of the select electrodes and an associated control input of one of the at least two drive switches (Column 4, Lines 23-25, "Switch **42** further includes a second transistor **50** having a current carrying terminal **51** connected to a gate or control terminal **52** of transistor **43**." The select transistor conveys the current to the drive transistor of the sub-pixels.), and

in that the control driver is adapted for supplying the control signals (DA) via at least two of the control electrodes to associated control inputs of the plurality of select switches. (Figure 3 shows the data driver which is responsible for this input and is sent to the sub-pixels **45-47**.)

Shieh teaches in Claim 7:

A method of driving an active matrix display comprising a matrix of display pixels being associated with intersections of crossing select electrodes and control electrodes (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix"), the method comprising

supplying a select signal (SE) to the select electrodes (Figure 3, the shift register scan driver **57** sends the select electrodes),

supplying a control signal (DA) to the control electrodes (Figure 3, the data driver **55** supplies the data signals.),

generating a plurality of different voltage levels (VBi) with a voltage generator (Figure 5 shows the multi-step voltage waveforms for each of RGB, Figure 3 shows the voltage generator 60), and supplying a selected one of said plurality of different voltage levels (VBi) via at least one voltage level electrode to an associated one of the display pixels (Figure 3 shows three voltage electrodes for each of the sub-pixels **45**, **46** and **47**) in dependence on both the select signal (SE) indicating whether the associated one of the pixels is selected and a control signal (CG) being applied to said voltage level generator (Figure 3 shows a signal being sent from the timing circuit 65 to voltage source 60 to select the appropriate voltage (Columns 3-4, Lines 65-8

) to indicate which one of said plurality of different voltage levels (VBi) has to be supplied to the associated one of the pixels. (Column 6, Lines 7-12, "In the multi-step voltage waveform of FIG. 5, one complete frame is illustrated. Each frame is divided into three subframes Vr, Vg, and Vb and each subframe is divided into m multi-steps of voltage or sub-subframes. As described previously, the multi-step subframe Vr is applied to the Vr output of voltage source 60 and the entire **matrix** is addressed for each of the m steps. This procedure is continued until all m of the sub-subframes are completed, completing a subframe." The matrix setup uses information from both the select and control electrodes.)

Shieh teaches in Claim 8:

A display apparatus with an active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") comprising

a matrix of display pixels being associated with intersections of crossing select electrodes and control electrodes (Figure 3 shows the setup for one pixel in a matrix),

a signal processing circuit for receiving an input display signal (VI) and for supplying a first control signal (CC), a second control signal (CS), and a third control signal (CG) (Figure 3 shows the timing circuit **65** which sends signals to the data driver **55**, the shift register scan **57** and the voltage source **60**),

a select driver for supplying select signals (SE) to the select electrodes under control of the first control signal (CS) (Figure 3, the shift register scan driver **57** sends the select electrodes),

a control driver for supplying control signals (DA) to the control electrodes under control of the second control signal (CC) (Figure 3, the data driver **55** supplies the data signals.),

a voltage level generator for generating a plurality of different voltage levels (VBi) under control of the third control signal (CG) (Figure 3 shows the voltage source **60** with terminals V_R, V_G, and V_B),

select circuits (Figure 3, switch **42**), each being coupled between an associated one of the display pixels and the voltage level generator, for supplying a selected one of said plurality of different voltage levels (VBi) (Figure 5 shows the multi-step voltage waveforms for each of RGB) to the associated one of the display pixels in dependence on both the select signals (SE) indicating whether the associated one of the pixels is selected and a control signal (CG) being applied to said voltage level generator (Figure 3 shows a signal being sent from the timing circuit 65 to voltage source 60 to select the appropriate voltage (Columns 3-4, Lines 65-8) to indicate which one of said plurality of different voltage levels (VBi) has to be supplied to the associated one of the pixels. (Column 6, Lines 7-12, "In the multi-step voltage waveform of FIG. 5, one complete frame is illustrated. Each frame is divided into three subframes Vr, Vg, and Vb and each subframe is divided into m multi-steps of voltage or sub-subframes. As described previously, the multi-step subframe Vr is applied to the Vr output of voltage source 60 and the entire **matrix** is addressed for each of the m steps. This procedure is continued until all m of the sub-subframes are completed, completing a subframe." The matrix setup uses information from both the select and control electrodes.)

Claim Rejections – 35 USC § 103

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claim 6** rejected under 35 U.S.C. 103(a) as being unpatentable over **Shieh et al. (5,748,160)** in view of **Katase (US 6,762,744 B2)**

Shieh teaches in Claim 6:

An active matrix display (Column 2, Lines 55-57, "Further, light emitting diode **10**, and each other diode in the matrix has a semiconductor switch **12** attached thereto, making the matrix an active matrix") as claimed in claim 1, but

Shieh does not explicitly teach that the display is "characterized in that the pixels comprise electrophoretic material."

However, in the same field of endeavor, display devices, Katase teaches "As stated above, the object of the present invention is to provide an **active matrix electrophoretic display**. Also provided is a drive circuit integral to the device, and a method for driving the display by using the circuit." (Column 1, Lines 40-43)

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the use of an electrophoretic display as taught by Katase with Shieh's display driving method with the motivation that "prior art electrophoretic displays suffer from a problem in that they afford poor viewing characteristics. The present invention has been made to overcome this problem, and provides for the first time an active matrix electrophoretic display, which display has superior viewing characteristics. (Column 1, Lines 31-35)

Response to Arguments

6. Applicant's arguments considered, but are considered, but are not found to be persuasive.

Shieh teaches in Figure 3 of a timing circuit 65 which sends signals to the data driver 55, shift register scan 57 and the voltage source 60. The signal to the voltage source is interpreted as control signal CG and determines which one of the plurality of different voltages levels and types are applied to the pixels.

Conclusions

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

AMR A. AWAD
SUPERVISORY PATENT EXAMINER